**16LF1784 Support Information**

**#pragma config Usage**

**#pragma config <setting>=<named value>**

For example:  
// Data Memory Code Protection: Data memory code protection is disabled  
// Brown-out Reset Enable: Brown-out Reset disabled  
// Internal/External Switchover: Internal/External Switchover mode is disabled  
// Oscillator Selection: ECM, External Clock, Medium Power Mode (0.5-4 MHz): device clock supplied to CLKIN pin  
// Fail-Safe Clock Monitor Enable: Fail-Safe Clock Monitor is disabled  
// MCLR Pin Function Select: MCLR/VPP pin function is digital input  
// Watchdog Timer Enable: WDT disabled  
// Flash Program Memory Code Protection: Program memory code protection is disabled  
// Power-up Timer Enable: PWRT disabled  
// Clock Out Enable: CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin  
#pragma config CPD = OFF, BOREN = OFF, IESO = OFF, FOSC = ECM, FCMEN = OFF, MCLRE = OFF, WDTE = OFF, CP = OFF, PWRTE = OFF, CLKOUTEN = OFF

**#pragma config <setting>=<literal constant>**

For example:  
// Data Memory Code Protection: Data memory code protection is disabled  
// Brown-out Reset Enable: Brown-out Reset disabled  
// Internal/External Switchover: Internal/External Switchover mode is disabled  
// Oscillator Selection: ECM, External Clock, Medium Power Mode (0.5-4 MHz): device clock supplied to CLKIN pin  
// Fail-Safe Clock Monitor Enable: Fail-Safe Clock Monitor is disabled  
// MCLR Pin Function Select: MCLR/VPP pin function is digital input  
// Watchdog Timer Enable: WDT disabled  
// Flash Program Memory Code Protection: Program memory code protection is disabled  
// Power-up Timer Enable: PWRT disabled  
// Clock Out Enable: CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin  
#pragma config CPD = 0x1, BOREN = 0x0, IESO = 0x0, FOSC = 0x6, FCMEN = 0x0, MCLRE = 0x0, WDTE = 0x0, CP = 0x1, PWRTE = 0x1, CLKOUTEN = 0x1

**#pragma config <register>=<literal constant>**

For example:   
// Data Memory Code Protection: Data memory code protection is disabled  
// Brown-out Reset Enable: Brown-out Reset disabled  
// Internal/External Switchover: Internal/External Switchover mode is disabled  
// Oscillator Selection: ECM, External Clock, Medium Power Mode (0.5-4 MHz): device clock supplied to CLKIN pin  
// Fail-Safe Clock Monitor Enable: Fail-Safe Clock Monitor is disabled  
// MCLR Pin Function Select: MCLR/VPP pin function is digital input  
// Watchdog Timer Enable: WDT disabled  
// Flash Program Memory Code Protection: Program memory code protection is disabled  
// Power-up Timer Enable: PWRT disabled  
// Clock Out Enable: CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin  
#pragma config CONFIG1 = 0xC9A6  
  
For example:   
// IDLOC @ 0x8000  
#pragma config IDLOC0 = 0x3FFF

**#pragma config Settings**

**Register: CONFIG1 @ 0x8007**

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| **CPD =** | **Data Memory Code Protection** |
| OFF | Data memory code protection is disabled |
| ON | Data memory code protection is enabled |

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| **BOREN =** | **Brown-out Reset Enable** |
| OFF | Brown-out Reset disabled |
| ON | Brown-out Reset enabled |
| NSLEEP | Brown-out Reset enabled while running and disabled in Sleep |
| SBODEN | Brown-out Reset controlled by the SBOREN bit in the BORCON register |

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| **IESO =** | **Internal/External Switchover** |
| OFF | Internal/External Switchover mode is disabled |
| ON | Internal/External Switchover mode is enabled |

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| **FOSC =** | **Oscillator Selection** |
| ECM | ECM, External Clock, Medium Power Mode (0.5-4 MHz): device clock supplied to CLKIN pin |
| XT | XT Oscillator, Crystal/resonator connected between OSC1 and OSC2 pins |
| LP | LP Oscillator, Low-power crystal connected between OSC1 and OSC2 pins |
| EXTRC | EXTRC oscillator: External RC circuit connected to CLKIN pin |
| ECH | ECH, External Clock, High Power Mode (4-32 MHz): device clock supplied to CLKIN pin |
| ECL | ECL, External Clock, Low Power Mode (0-0.5 MHz): device clock supplied to CLKIN pin |
| INTOSC | INTOSC oscillator: I/O function on CLKIN pin |
| HS | HS Oscillator, High-speed crystal/resonator connected between OSC1 and OSC2 pins |

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| **FCMEN =** | **Fail-Safe Clock Monitor Enable** |
| OFF | Fail-Safe Clock Monitor is disabled |
| ON | Fail-Safe Clock Monitor is enabled |

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| **MCLRE =** | **MCLR Pin Function Select** |
| OFF | MCLR/VPP pin function is digital input |
| ON | MCLR/VPP pin function is MCLR |

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| **WDTE =** | **Watchdog Timer Enable** |
| OFF | WDT disabled |
| ON | WDT enabled |
| NSLEEP | WDT enabled while running and disabled in Sleep |
| SWDTEN | WDT controlled by the SWDTEN bit in the WDTCON register |

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| **CP =** | **Flash Program Memory Code Protection** |
| OFF | Program memory code protection is disabled |
| ON | Program memory code protection is enabled |

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| **PWRTE =** | **Power-up Timer Enable** |
| OFF | PWRT disabled |
| ON | PWRT enabled |

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| **CLKOUTEN =** | **Clock Out Enable** |
| OFF | CLKOUT function is disabled. I/O or oscillator function on the CLKOUT pin |
| ON | CLKOUT function is enabled on the CLKOUT pin |

**Register: CONFIG2 @ 0x8008**

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| **LPBOR =** | **Low Power Brown-Out Reset Enable Bit** |
| OFF | Low power brown-out is disabled |
| ON | Low power brown-out is enabled |

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| **PLLEN =** | **PLL Enable** |
| OFF | 4x PLL disabled |
| ON | 4x PLL enabled |

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| **WRT =** | **Flash Memory Self-Write Protection** |
| OFF | Write protection off |
| BOOT | 000h to 1FFh write protected, 200h to FFFh may be modified by EECON control |
| HALF | 000h to 7FFh write protected, 800h to FFFh may be modified by EECON control |
| ALL | 000h to FFFh write protected, no addresses may be modified by EECON control |

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| **STVREN =** | **Stack Overflow/Underflow Reset Enable** |
| OFF | Stack Overflow or Underflow will not cause a Reset |
| ON | Stack Overflow or Underflow will cause a Reset |

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| **BORV =** | **Brown-out Reset Voltage Selection** |
| LO | Brown-out Reset Voltage (Vbor), low trip point selected. |
| HI | Brown-out Reset Voltage (Vbor), high trip point selected. |

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| **LVP =** | **Low-Voltage Programming Enable** |
| OFF | High-voltage on MCLR/VPP must be used for programming |
| ON | Low-voltage programming enabled |

**Register: IDLOC0 @ 0x8000**

**Register: IDLOC1 @ 0x8001**

**Register: IDLOC2 @ 0x8002**

**Register: IDLOC3 @ 0x8003**